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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,803	09/11/2003	**William C. Black**	X-1356 US	5248

24309 7590 03/21/2008

XILINX, INC
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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
03/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,803	BLACK ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/17/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 16-23* is/are pending in the application.

4a) Of the above claim(s) *9-15 and 24-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,16,17 and 19* is/are rejected.

7)☒ Claim(s) *3,5-8,18 and 20-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Election Requirement

1. The response to Election Requirement filed on 12/17/2007 has been entered. Group II (claims 1-8 and 16-23) has been elected.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4, 16, 17 and 19 are rejected under 35 U.S.C. 102(e) as anticipated by Benyamin et al. (US 6,531,931) and Shirani et al. (US 6,188,721) (Where as described in column 1 lines 8-20, the Shirani et al. (US 6,188,721) reference is incorporated by reference by the Benyamin et al. (US 6,531,931) reference).

- With regard claim 1, Benyamin et al. discloses an analog front-end (Fig.1 element 115) having built-in equalization (Fig.1 element 310), the analog front-end comprises:

  control module (Fig.1 element 405) operably coupled to provide a frequency response setting (Fig.1 element 415, Fig.2 elements 125 and 415 and Fig.8 , and column 9 lines 30-43, where Filter Select 415, selects on of the two

different High Pass filters from Fig.8 to provide a frequency response setting) based on a channel response of a channel (column 9, lines 30-43, where the channel response is determined by the cable length. i.e. the channel response of the short cable is different from that of a long cable. when the channel response with respect to short cable, Filter Select 415 selects three pole/zero high pass filter and when the channel response with respect to long cable, Filter Select 415 selects two pole/zero high pass filter.) providing high-speed serial data to the analog front end; and

tunable gain stage (Fig.1 and Fig.2, element 310) operably coupled to amplify and equalize the high-speed serial data (Shirani's reference, column 3 lines 47-54) based on the frequency response setting, wherein the tunable gain stage includes:

a frequency dependent load that is adjusted based on the frequency response setting (Fig.8 and column 9 line 30 – column 10 line 19, where the first frequency dependent load, three pole high pass filter, is formed by C1, C4, C5, R3-R9 with respect to the short cable channel response (column 9 lines 44-67) and the second frequency dependent load, two pole high pass filter, is formed by C1- C3, C6, R3, R5, R10 and R11 with respect to the long cable channel response (column 10 lines 1-19)); and

amplifier input section operably coupled to the frequency dependent load (Fig.2 elements 315 and 317, 212 and 213 and Fig.8 elements 212 and 213, where the amplifier input 315 and 317 couples to the frequency dependent load

via DC amplifier multiplier stage 120 and AC/DC gain stage 125 and the gain of the AC/DC gain stage 125 is determined by the two frequency dependent loads, respectively, as described in column 9 line 65 and column 10 line 15),

wherein the amplifier input section receives the high-speed serial data (Fig.1 element 105) and, in conjunction with the frequency dependent load (column 9 line 30 – column 10 line 19) amplifies and equalizes the high-speed serial data to produce an amplified and equalized serial data (Fig.1 and Fig.2 element 325).

- With regard claim 2, Benyamin et al. further discloses wherein the tunable gain stage further comprises:

a first stage (Fig.2 element 125) operably coupled to amplify and equalize, to a first level, the high-speed serial data based on the frequency response setting (Fig.1 element 415, Fig.2 elements 125 and 415 and Fig.8, and column 9 lines 30-43, where Filter Select 415, selects on of the two different High Pass filters from Fig.8 to provide a frequency response setting) to produce a first amplified and equalized serial data (Fig.2 element 125 outputs); and

a second stage (Fig.2 element 135) operably coupled to amplify and equalize the first amplified and equalized serial data (Fig.2 element 125 outputs) based on the frequency response setting (Fig.1 element 415, Fig.2 elements 125 and 415 and Fig.8, and column 9 lines 30-43, where Filter Select 415, selects on of the two different High Pass filters from Fig.8 to provide a frequency response

setting) to produce the amplified and equalized serial data (Fig.1 and Fig.2 element 325).

- With regard claim 4, Benyamin et al. further discloses wherein the frequency dependent load further comprises at least one high pass filter (Fig.8 and column 9 line 30 – column 10 line 19, where the first frequency dependent load, three pole high pass filter, is formed by C1, C4, C5, R3-R9 with respect to the short cable channel response (column 9 lines 44-67) and the second frequency dependent load, two pole high pass filter, is formed by C1- C3, C6, R3, R5, R10 and R11 with respect to the long cable channel response (column 10 lines 1-19)).
- With regard claim 16, Benyamin et al. further discloses a clock and data recovery module operably coupled to recover a clock signal and data from the amplified and equalized high-speed data (Shirani's reference, column 7 lines 5-17 and column 31 lines 29-41, where Shirani teaches a clock recovery circuit. In further, Benyamin's equalization amplifier and equalizer circuit (Fig.1 element 310) is a data recovery circuit that compensates the short cable and long cable loss (column 10 line 28-62). It is clear that Benyamin et al. teach a data recovery circuit as addressed in the above paragraph.)

  All other limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 17, which is a receiver claim related to claim 2, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.

- With regard claim 19, which is a receiver claim related to claim 4, all limitation is contained in claim 4. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

4. Claims 3, 5-8, 18 and 20-23 are objected to as being dependent upon an objected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ted M Wang/
Primary Examiner, Art Unit 2611